The Transformerless Single-Phase Universal Active Power Filter for Harmonic and Reactive Power Compensation

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***Abstract*—This paper presents a universal active filter for harmonic and reactive power compensation for single-phase systems applications. The proposed system is a combination of parallel and series active filters without transformer. It is suitable for applications where size and weight are critical factors. The model of the system is derived and it is shown that the circulating current observed in the proposed active filter is an important quantity that must be controlled. A complete control system, including pulse-width modulation (PWM) techniques, is developed. Comparisons between the structures are made from weighted total harmonic distortion (WTHD). The steady-state analysis is also presented in order to demonstrate the possibility to obtain an optimum voltage angle reducing the current amplitude of both series and parallel converters and, consequently, the total losses of the system. Simulated and experimental results validate the theoretical considerations.**

***Index Terms*—Optimum voltage angle, single-phase configuration, total harmonic distortion, universal active power filter (UAPF).**

I. Introduction

THE strict requirement of power quality at input ac mains and the output load (sensitive loads) in the area of power line conditioning is very important in power electronics [1]. Different equipments are used to improve the power quality, e.g., transient suppressors, line voltage regulators, uninterrupted power supplies, active filters, and hybrid filters [1]–[6]. The continuous proliferation of electronic equipment either for home appliance or industrial use has the drawback of increasing the nonsinusoidal current into power network. Thus, the need for economical power conditioners for single-phase systems is growing rapidly [2], [7]–[12]. Different mitigation solutions are currently proposed and used in practice applications to work out the problems of harmonics in electric grids. Over the past few decades, the use of active filtering techniques has became more attractive due to the technological progress in power electronic switching devices, enhanced numerical methods, and more efficient control algorithms.

The series active power filter (SAPF) [13]–[18] provides load voltage control eliminating voltage disturbances, such as unbalance, sags, notches, flickers, and voltage harmonics, so that a regulated fundamental load voltage with constant magnitude is provided to the load. The purpose of a parallel active power filter (PAPF) [19]–[31] is to absorb harmonic currents, compensate for reactive power, and regulate the dc-bus voltage between both active filters. The universal active power filter (UAPF) [32]–[43] which is a combination of both, is a versatile device that operates as series and parallel active power filter. It can simultaneously fulfill different objectives like maintaining a sinusoidal voltage (harmonic free) at the load, source current harmonics elimination, load balance, and power factor correction. For standard configuration [see Fig. 1(a)], the series converter utilizes a transformer for isolation. The cost and size associated with the transformer makes undesirable such a solution, mainly for office and home environments.

This paper proposes an universal active filter topology for single-phase systems applications without transformer, as shown in Fig. 1(b). In this case, the control of the circulating current becomes an important aspect in the converter design because this current may contribute to additional power loss and large circulating current may cause severe instability and also make damage to the circuit devices. A complete control system, including pulse-width modulation (PWM) techniques, is developed. Comparisons between the structures are made from weighted total harmonic distortion (WTHD). The steady-state analysis is also presented in order to demonstrate the possibility to obtain an optimum voltage angle reducing the current amplitude of both series and parallel converters and, consequently, the total losses of the system. The operation principle, control strategy, steady-state analysis, simulated, and experimental results are presented to validate the theoretical considerations.

II. System Model

The proposed configuration shown in Fig. 1(b) comprise the grid (e_g, i_g), internal grid inductance (L_g), load Z_l (v_l, i_l),

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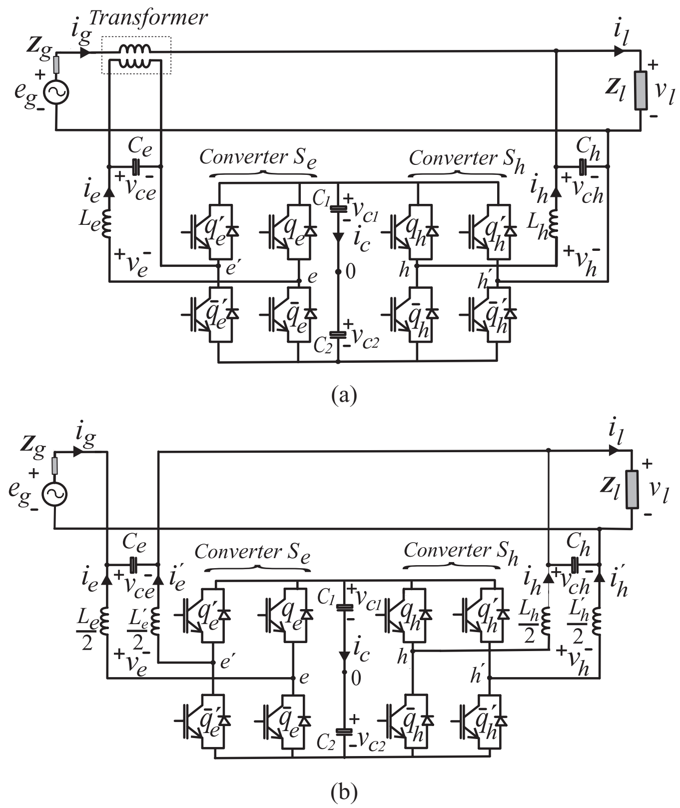


Fig. 1. Single-phase UAPF: (a) conventional structure and (b) transformerless proposed structure.

converters S_e and S_h with a capacitor bank at the dc-link and filters Z_e (L_e, L'_e, and C_e) and Z_h (L_h, L'_h and C_h). Converter S_e is composed of switches q_e, $\overline{q}_e$, q'_e, and $\overline{q}'_e$. Converter S_h is composed of switches q_h, $\overline{q}_h$, q'_h, and $\overline{q}'_h$. The conduction state of all switches is represented by an homonymous binary variable, where $q = 1$ indicates a closed switch, while $q = 0$ an open one. The converter pole voltages v_{e0}, v'_{e0}, v_{h0}, and v'_{h0} depend on the conduction states of the power switches, that is

$$v_{e0} = (2q_e - 1)\frac{v_c}{2} \tag{1}$$

$$v'_{e0} = (2q'_e - 1)\frac{v_c}{2} \tag{2}$$

$$v_{h0} = (2q_h - 1)\frac{v_c}{2} \tag{3}$$

$$v'_{h0} = (2q'_h - 1)\frac{v_c}{2} \tag{4}$$

where v_c is the dc-link voltage.

From Fig. 1(b), the following equations can be derived:

$$v_{e0} - v'_{e0} = \left(\frac{r_e}{2} + \frac{l_e}{2}p\right) i_e - \left(\frac{r'_e}{2} + \frac{l'_e}{2}p\right) i'_e + v_g - v_l \tag{5}$$

$$v_{h0} - v'_{h0} = \left(\frac{r_h}{2} + \frac{l_h}{2}p\right) i_h - \left(\frac{r'_h}{2} + \frac{l'_h}{2}p\right) i'_h + v_l \tag{6}$$

$$v'_{e0} - v'_{h0} = \left(\frac{r'_e}{2} + \frac{l'_e}{2}p\right) i'_e - \left(\frac{r'_h}{2} + \frac{l'_h}{2}p\right) i'_h + v_l \tag{7}$$

$$v_{e0} - v_{h0} = \left(\frac{r_e}{2} + \frac{l_e}{2}p\right) i_e - \left(\frac{r_h}{2} + \frac{l_h}{2}p\right) i_h + v_g - v_l \tag{8}$$

$$e_g - v_{ce} - v_l = (r_g + l_g p)\, i_g \tag{9}$$

$$pv_{ce} = \frac{1}{C_e}(i_g + i_e) \tag{10}$$

$$pv_l = \frac{1}{C_h}(i_g - i_l - i'_h) \tag{11}$$

where $p = d/dt$, $v_g = e_g - r_g i_g - l_g p i_g$, $v_l = v_{ch}$, and i_l is calculated using the load model which can be linear or nonlinear; and symbols r and l represent resistances and inductances of the inductors L_g, L_e, L'_e, L_h, and L'_h. The circulating current i_o is defined by

$$i_o = i_e + i'_e = -(i_h + i'_h). \tag{12}$$

The demonstration of (12) is presented in Appendix I. By introduction of i_o, (5)–(11) can be written as

$$\begin{aligned} v_{e0} - v'_{e0} = &\left[\frac{r'_e}{2} + \frac{r_e}{2} + \left(\frac{l_e}{2} + \frac{l'_e}{2}\right) p\right] i_e \\ &+ v_g - v_l - \left(\frac{r'_e}{2} + \frac{l'_e}{2}p\right) i_o \end{aligned} \tag{13}$$

$$\begin{aligned} v_{h0} - v'_{h0} = &\left[\frac{r_h}{2} + \frac{r'_h}{2} + \left(\frac{l_h}{2} + \frac{l'_h}{2}\right) p\right] i_h \\ &+ v_l + \left(\frac{r'_h}{2} + \frac{l'_h}{2}p\right) i_o \end{aligned} \tag{14}$$

$$\begin{aligned} v'_{e0} - v'_{h0} = &\left[\left(\frac{r'_e}{2} + \frac{r'_h}{2}\right) + \left(\frac{l'_e}{2} + \frac{l'_h}{2}\right) p\right] i_o + v_l \\ &- \left(\frac{r'_e}{2} + \frac{l'_e}{2}p\right) i_e + \left(\frac{r'_h}{2} + \frac{l'_h}{2}p\right) i_h \end{aligned} \tag{15}$$

$$v_{e0} - v_{h0} = \left(\frac{r_e}{2} + \frac{l_e}{2}p\right) i_e - \left(\frac{r_h}{2} + \frac{l_h}{2}p\right) i_h + v_g - v_l \tag{16}$$

$$e_g - v_{ce} - v_l = (r_g + l_g p) i_g \tag{17}$$

$$pv_{ce} = \frac{1}{C_e}(i_g + i_e) \tag{18}$$

$$pv_l = \frac{1}{C_h}(i_g - i_l + i_h + i_o). \tag{19}$$

The resultant circulating voltage model is obtained by adding (13)–(16)

$$\begin{aligned} v_o &= v'_{e0} + v_{e0} - v'_{h0} - v_{h0} \\ &= \left[\left(\frac{r'_e}{2} + \frac{r'_h}{2}\right) + \left(\frac{l'_e}{2} + \frac{l'_h}{2}\right) p\right] i_o \\ &\quad + \left[\left(\frac{r_e}{2} - \frac{r'_e}{2}\right) + \left(\frac{l_e}{2} - \frac{l'_e}{2}\right) p\right] i_e \\ &\quad - \left[\left(\frac{r_h}{2} - \frac{r'_h}{2}\right) + \left(\frac{l_h}{2} - \frac{l'_h}{2}\right) p\right] i_h + v_g. \end{aligned} \tag{20}$$

The voltage v_o is used to compensate for the circulating current i_o.

The final model is then composed of (13), (14), (17)–(19), and (20). Given the variables e_g and i_l (defined by load model), v_{e0}, v'_{e0}, v_{h0}, and v'_{h0}, variables i_g, i_e, i_h, i_o, v_l, and v_{ce} can be determined from this model.

From the point of view of the controllers, the voltages: $v_e = v_{e0} - v'_{e0}$ (converter S_e) is used to regulate and compensate for the load voltage v_l, $v_h = v_{h0} - v'_{h0}$ (converter S_h) regulates and controls the grid current in order to maintain the power factor close to one and $v_o = v'_{e0} + v_{e0} - v'_{h0} - v_{h0}$ (converter $S_e + S_h$) is used to cancel or maintain the circulating current i_o near to zero.

In the balanced case, filter inductors are equal ($L_e = L'_e$ and $L_h = L'_h$) the circulating voltage model becomes

$$v_o = v_g + \left[\left(\frac{r_e}{2} + \frac{r_h}{2}\right) + \left(\frac{l_e}{2} + \frac{l_h}{2}\right)p\right] i_o. \tag{21}$$

Thus, it can be noted that to minimize the circulating current i_o, the voltage v_o must be equal to v_g, i.e,

$$v_o = v_g \tag{22}$$

When $i_o = 0$ ($i_e = -i'_e$, $i_h = -i'_h$), the system model becomes

$$v_{e0} - v'_{e0} = v_g + (r_e + l_e p)i_e - v_l \tag{23}$$

$$v_{h0} - v'_{h0} = (r_h + l_h p)i_h + v_l \tag{24}$$

$$e_g - v_{ce} - v_l = (r_g + l_g p)i_g \tag{25}$$

$$pv_{ce} = \frac{1}{C_e}(i_g + i_e) \tag{26}$$

$$pv_l = \frac{1}{C_h}(i_g - i_l + i_h). \tag{27}$$

This model is similar to the model of the conventional filter with an ideal transformer. Therefore, we can use $v_e = v_{e0} - v'_{e0}$ (converter S_e) to regulate the load voltage and $v_h = v_{h0} - v'_{h0}$ (converter S_h) to control the power factor and harmonics of i_g as in the conventional filter.

III. PWM Strategy

The PWM strategy of the converters can be directly calculated from the pole voltages $v^{*\prime}_{e0}$, v^*_{e0}, $v^{*\prime}_{h0}$, and v^*_{h0}. Considering that v^*_e, v^*_h, and v^*_o denote the reference voltages requested by the controllers (see Section VI), it comes

$$v^*_{e0} - v^{*\prime}_{e0} = v^*_e \tag{28}$$

$$v^*_{h0} - v^{*\prime}_{h0} = v^*_h \tag{29}$$

$$v^{*\prime}_{e0} + v^*_{e0} - v^{*\prime}_{h0} - v^*_{h0} = v^*_{o.} \tag{30}$$

These equations are insufficient to determine the four pole voltages v^*_{e0}, $v^{*\prime}_{e0}$, v^*_{h0}, and $v^{*\prime}_{h0}$. Introducing an auxiliary variable v^*_x and choosing $v^{*\prime}_{e0} = v^*_x$, it can be written as

$$v^*_{e0} = v^*_e + v^*_x \tag{31}$$

$$v^{*\prime}_{e0} = v^*_x \tag{32}$$

$$v^*_{h0} = \frac{v^*_e}{2} + \frac{v^*_h}{2} - \frac{v^*_o}{2} + v^*_x \tag{33}$$

$$v^{*\prime}_{h0} = \frac{v^*_e}{2} - \frac{v^*_h}{2} - \frac{v^*_o}{2} + v^*_x. \tag{34}$$

Two methods are presented next in order to choose v^*_x.

Method A: General approach

In this manner, the reference voltage v^*_x is calculated by taking into account the maximum $v^*_c/2$ and minimum $-v^*_c/2$ value of the pole voltages, then

$$v^*_{x\max} = v^*_c/2 - v^*_{\max} \tag{35}$$

$$v^*_{x\min} = -v^*_c/2 - v^*_{\min} \tag{36}$$

where v^*_c is the reference dc-link voltages, $v^*_{\max} = \max\vartheta$ and $v^*_{\min} = \min\vartheta$ with $\vartheta = \{v^*_e, 0, v^*_e/2 + v^*_h/2 - v^*_o/2, v^*_e/2 - v^*_h/2 - v^*_o/2\}$.

After v^*_x is selected, all pole voltages are obtained from (31)–(34). Then, v^*_x can be chosen equal to $v^*_{x\max}$, $v^*_{x\min}$, or $v^*_{x\text{avg}} = (v^*_{x\max} + v^*_{x\min})/2$. Note that when $v^*_{x\max}$ or $v^*_{x\min}$ is selected, one of the converter-leg operates with zero switching frequency. On the other hand, operation with $v^*_{x\text{ave}}$ generates pulse voltage centered in the sampling period that can improve the THD of voltages.

The maximum and minimum values can be alternatively used. For example, during the time interval τ choose $v^*_x = v^*_{x\max}$ and in the next choose $v^*_x = v^*_{x\min}$. The interval τ can be made equal to the sampling period (the smallest value) or multiple of the sampling period to reduce the average switching frequency.

Once v^*_x is chosen, pole voltages $v^{*\prime}_{e0}$, v^*_{e0}, $v^{*\prime}_{h0}$, and v^*_{h0} are defined from (31)–(34). Since the pole voltages have been defined, pulse-widths τ_e, τ'_e, τ_h, and τ'_h can be calculated by

$$\tau_e = \frac{T}{2} + \frac{T}{v_c}v^*_{e0} \tag{37}$$

$$\tau'_e = \frac{T}{2} + \frac{T}{v_c}v^{*\prime}_{e0} \tag{38}$$

$$\tau_h = \frac{T}{2} + \frac{T}{v_c}v^*_{h0} \tag{39}$$

$$\tau'_h = \frac{T}{2} + \frac{T}{v_c}v^{*\prime}_{h0}. \tag{40}$$

Alternatively, the gating signals can be generated by comparing the pole voltage with a high-frequency triangular carrier signal.

Method B: Local approach

In this case, the voltage v^*_{xs} is calculated by taking into account its maximum and minimum values in the series or shunt side. For example, if the series side is considered ($s = e$), then $v^*_{xe\max} = \max\vartheta_e$ and $v^*_{xe\min} = \min\vartheta_e$ with $\vartheta_e = \{v^*_e, 0\}$ and if the shunt side ($s = h$) is considered, then $v^*_{xh\max} = \max\vartheta_h$ and $v^*_{xh\min} = \min\vartheta_h$ with $\vartheta_h = \{v^*_e/2 + v^*_h/2 - v^*_o/2, v^*_e/2 - v^*_h/2 - v^*_o/2\}$. Besides these voltages, voltage v^*_x must also obey the other converter side.Then, these limits can be obtained directly from $v^*_{x\max}$ and $v^*_{x\min}$from (35) and (36).

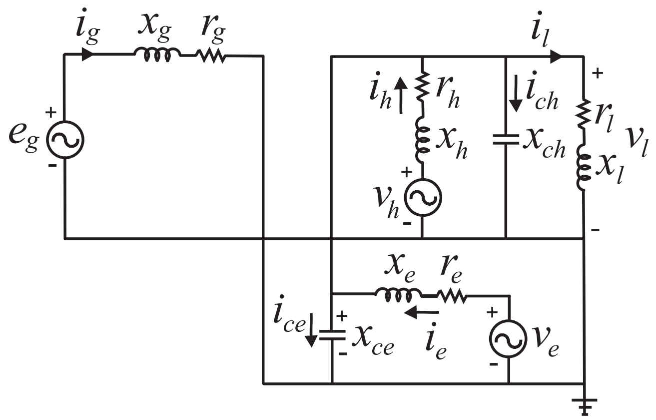


Fig. 2. Steady-state circuit of the single-phase universal active filter without transformer.

TABLE I
PARAMETERS OF THE TRANSFORMERLESS UAPF—VALUES IN P.U.

$\|e_g\|$	$\|v_l\|$	PF	r_g	r_e	r_h	x_g	x_e	x_h	x_{ce}	x_{ch}
1.0	1.0	0.85 lag	0.001	0.005	0.005	0.01	0.05	0.05	1.0	1.0

The algorithm for this case is given by

1) Choose the converter side to be the THD optimized and calculate v_{xs}^* between $v_{xs\max}^*$, $v_{xs\min}^*$, or $v_{xs\text{ave}}^* = (v_{xs\max}^* + v_{xs\min}^*)/2$.
2) Calculate the limits $v_{x\max}^*$ and $v_{x\min}^*$ from (35) and (36).
3) Do $v_{xs}^* = v_{x\max}^*$ if $v_{xs}^* > v_{x\max}^*$ and $v_{xs}^* = v_{x\min}^*$ if $v_{xs}^* < v_{x\min}^*$.
4) Do $v_x^* = v_{xs}^*$.
5) Determine the pole voltage and the gating signal as in previous method.

IV. Optimization of the Voltage Load Angle

The steady-state analysis of the proposed active filter is based on the circuit presented in Fig. 2. The phasor equations that describe the behavior of the proposed system are obtained in the complex form. In Fig. 2 is presented the grid (E_g and I_g), internal grid impedance (r_g and x_g), series voltage (V_e), series impedance (r_e, x_e and x_{ce}), series current (I_e), parallel voltage (V_h), parallel impedance (r_h, x_h, and x_{ch}), parallel current (I_h), and load impedance (r_l, x_l). Table I contains the parameters in p.u. used for the steady-state simulations. The power load S_l presents a inductive power factor (PF) equal to 0.85. The simulation results showing the behavior of the converter voltages are presented in Figs. 3 and 4.

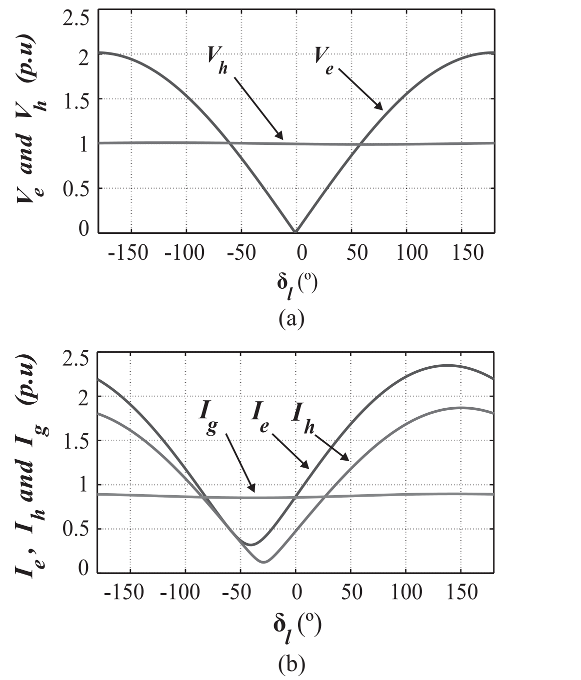


Fig. 3. Steady-state analysis of the single-phase universal active filter without transformer: (a) converter voltages and (b) converter currents and grid current.

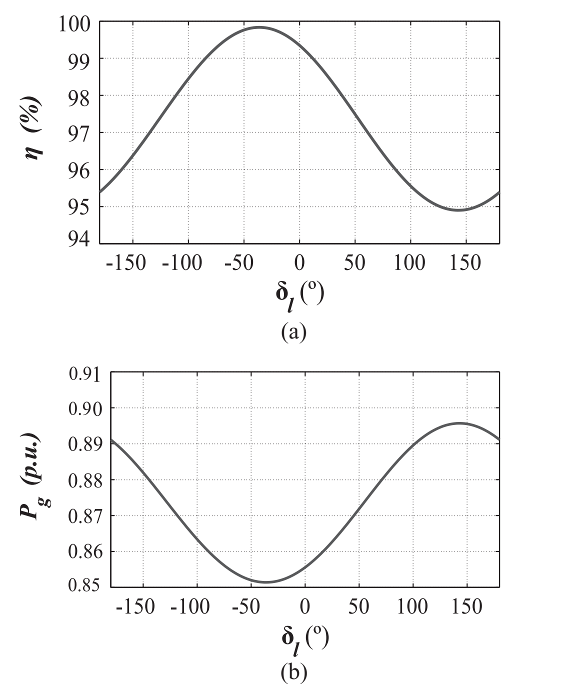


Fig. 4. Steady-state analysis of the single-phase universal active filter without transformer: (a) efficiency and (b) power of the ac grid.

It is observed in the Fig. 3(a) the behavior of the voltages converter as a function of the load angle δ_l (phase angle between the grid voltage e_g and the load voltage v_l). The voltage amplitude of the series converter increases considerably as δ_l moves away from $\delta_l \approx -4°$, which is the point of smallest voltage amplitude. The amplitudes of currents in the series (I_e) and parallel (I_h) converters and in the grid (I_g) are shown in Fig. 3(b). It can be seen that currents I_e and I_h assume the smallest values for $\delta_l \approx -40°$ and $\delta_l \approx -30°$, respectively. The grid current remains constant.

The point of higher efficiency of the system is located in $-50° < \delta_l < -25°$, as shown in Fig. 4(a), in which I_e and I_h have the smallest values resulting in the smallest converter losses; see Fig. 3(b). Also, it was observed from simulation that the point of larger efficiency corresponds to that of the smallest power delivered by grid, that is, $\delta_l \approx -36°$. This allows choosing the best angle δ_l in order to optimize the system operation. The efficiency η and the power of the ac grid are presented in Fig. 4. It is observed that the point of higher efficiency is the point where the grid provides the lowest ac power.

In voltage sources V_e and V_h which represent the voltages of converters S_e and S_h were not inserted the internal losses of the switches (IGBTs and diodes). The focal point of the steady-states analysis is to demonstrate that there is an optimum voltage angle δ_l which can decrease the amplitudes of converters' currents. It is clear that when the currents of the converters decrease the losses in the converters will also decrease; see Section VII.

In the steady-state analysis, it was considered the behavior of the frequency fundamental component and the load as RL with inductive power factor equal to 0.85. But if the load is nonlinear, it can determined the rms value of the load current signal with its corresponding phase shift.

V. Total Harmonic Distortion

Table II presents the WTHD values for the standard [see Fig. 1 (a)] and proposed [see Fig. 1(b)] configurations. The WTHD has been computed by using

$$\mathrm{WTHD}(p) = \frac{100}{a_1}\sqrt{\sum_{i=2}^{p}\left(\frac{a_i}{i}\right)^2} \tag{41}$$

where a_1 is the amplitude of the fundamental component, a_i is the amplitude of ith harmonic, and p is the number of harmonics taken into consideration.

The active filter parameters are calculated considering a rated load with different power factors and the number of harmonics taken into considerations is equal to $p = 1000$. In Table II is presented the $\mathrm{THD_e}$ (series converter) and $\mathrm{THD_h}$ (parallel converter) for the conventional configuration [see Fig. 1(a)] and for the proposed one [see Fig. 1(b)]. Results in Table II have been computed the WTHD for different load power factors (ϕ) and considering the PWM strategies (*Method A and Method B*). Furthermore, the WTHD of the circulating voltage (which is obtained from circulating current) has been addressed—$\mathrm{THD_o}$. The proposed configuration presents a small WTHD but its value is higher than that of conventional configuration. This is because of the need to compensate the circulating current i_o via voltage v_o. *Method B*—series (*Method B* - parallel) permits to reduce the WTHD in the series (parallel) converter side, but WTHD of v_o is higher than that obtained with *Method A*, as observed in Table II.

VI. Overall Control Strategy

Fig. 5 presents the control block diagram of the system. The capacitor dc-link voltage v_c ($v_c = E$) is adjusted to a reference value by using the controller R_c, which is a standard PI (proportional-integral) type controller. This controller provides the amplitude of the reference current I_g^*. For the power factor and harmonic control, the instantaneous reference current i_g^* must be synchronized with voltage e_g. This is performed by the block GEN-g, from a phase-locked loop (PLL) scheme. From the synchronization with e_g and the amplitude I_g^*, the current i_g^* is generated. The current controller is implemented by using the controller indicated by block R_i which the input reference voltage v_h^* used to compose the PWM strategies for grid's current compensation.

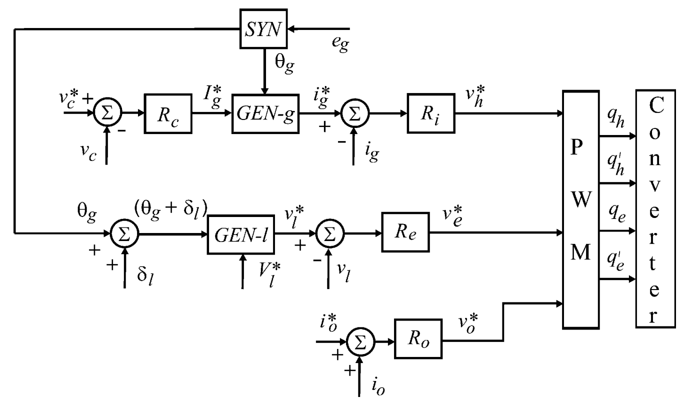


Fig. 5. Control block diagram.

The instantaneous reference load voltage v_l^* can be determined by using the rated optimized load angle δ_l plus the information θ_g from block SYN and the defined load amplitude V_l^*. The block GEN-l uses the input information to generate the desired reference load voltage v_l^*. From the difference between the voltages v_l^* and v_l the block of control defined as R_e generates the reference voltage signal v_e^* to be applied to the PWM strategies in order to to compensate for the load voltage.

The homopolar current i_o is controlled by controller R_o, that determines voltage v_o^* responsible to minimize the effect of the circulating current i_o, maintaining this current near to zero.

The controllers are of type double-sequence digital controllers employed in [44] and all these reference voltages v_h^*, v_e^*, and v_o^* are applied to the PWM block to determine the conduction states of the converter's switches.

VII. Simulated Results

The proposed configuration was simulated using PSIM software with the following circuit parameters:

1) Power system: 1.2 kVA;
2) Source frequency of e_g: 60 Hz;
3) Harmonic frequency of e_g: 180 Hz;
4) DC-bus voltage, v_c: 130 V_{dc} and 250 V_{dc};
5) Inductors filters, L_e and L_f: 7 mH;
6) Capacitor filter, C_e: 70 μF;
7) Grid voltage, e_g: 110 $V_{\mathrm{rms}} \pm 20\%$;
8) Grid voltage, e_g: 50 V_{rms} and 100 $V_{\mathrm{rms}} \pm 20\%$;
9) Load voltage, v_l: 50 V_{rms} and 100 V_{rms};
10) Linear load composed by: $R = 5\ \Omega$ and $L = 63$ mH.
11) Nonlinear load composed by diode bridge rectifier with: $R = 5\,\Omega$, $L = 75$ mH.

The proposed configurations does not use a transformer in the series connection and consist of four-leg converter. The capacitors of the dc-bus voltage and the switching frequency were, respectively, selected as $C = 2200\,\mu$F and 10 kHz.

TABLE II
WTHD FOR DIFFERENT POWER FACTOR ANGLES

	Standard		Proposed (*Method A*)			Proposed (*Method B* - series)			Proposed (*Method B* - parallel)		
ϕ	THD_e	THD_h	THD_e	THD_h	THD_o	THD_e	THD_h	THD_o	THD_e	THD_h	THD_o
-32^o	0.3877	0.3077	0.5192	0.4123	0.4096	0.4444	0.6155	0.6102	0.7254	0.3606	0.5946
-45^o	0.4226	0.2838	0.5502	0.3801	0.4569	0.4777	0.5732	0.6610	0.7588	0.3363	0.6248
-60^o	0.4557	0.2655	0.5805	0.3540	0.5108	0.5093	0.5395	0.7132	0.7814	0.3175	0.6521
-15^o	0.4239	0.3303	0.5582	0.4320	0.3809	0.4793	0.6586	0.5847	0.7701	0.3814	0.5656
0^o	0.4560	0.3333	0.5924	0.4323	0.3725	0.5094	0.6686	0.5808	0.8016	0.3840	0.5496

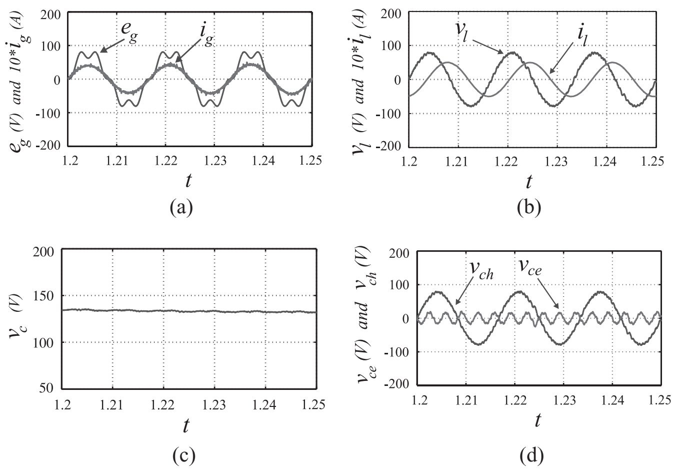


Fig. 6. Simulated results for a linear load: (a) voltage (e_g) and current (i_g) of the grid, (b) voltage (v_l) and current (i_l) of the load. (c) dc-bus voltage (v_c), (d) voltages v_{ce} and v_{ch}.

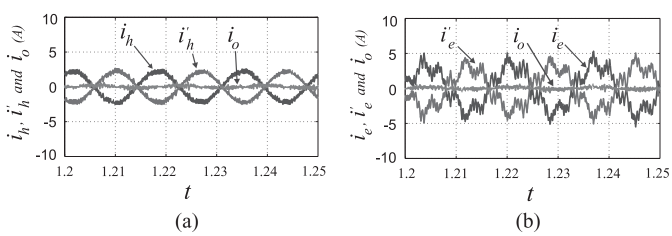


Fig. 7. Simulated results for a linear load: (a) currents of converter S_h (i_h and i'_h) and circulating current (i_o), (b) currents of converter S_e (i_e and i'_e) and circulating current (i_o).

In order to demonstrate the feasibility of the proposed configuration, two different kinds of simulated results are presented. The first one comprises a linear load and the other one is by nonlinear load. The *PWM* modulation method used to simulate the proposed configuration was the general approach (Method A). The difference between the methods A or B is that method B enables improving *WTHD* of series or parallel converter; see Section V.

The simulated results for linear load conditions as presented in Figs. 6 and 7. Fig. 6(a) shows the voltage and current of the grid, with power factor close to unit. At the grid voltage was inserted a disturbance of 20% of third harmonic. The voltage and current of the load are observed at Fig. 6(b). From presented results, it is noted that even with the presence of third harmonic at the grid, the load voltage and grid current remain sinusoidal with low harmonic distortion level. The dc-bus voltage shown in Fig. 6(c). Fig. 6 (d) presents the filters capacitors voltages $v_{ce} = e_g - v_l$ and $v_{ch} = v_l$.

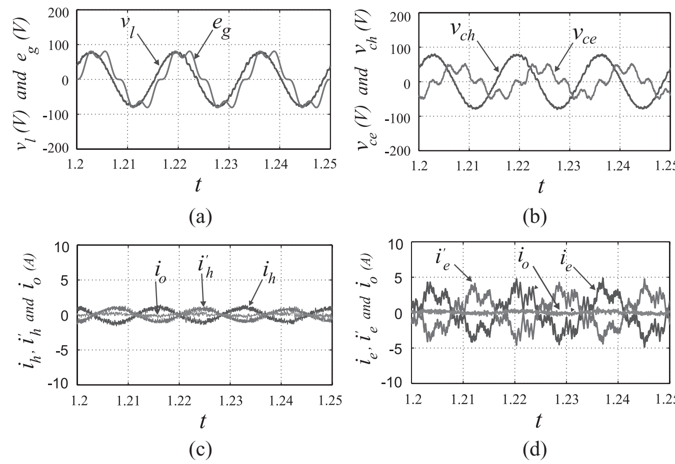


Fig. 8. Simulated results for a linear load with $\delta_l = -35°$: (a) load (v_l) and grid (e_g) voltage, (b) voltages of the filters capacitors v_{ce} and v_{ch}, (c) currents of converter S_h (i_h and i'_h) and circulating current (i_o), (d) currents of converter S_e (i_e and i'_e) and circulating current (i_o).

The circulating current i_o and converters' currents are shown at Fig. 7. The current i_o is composed of i_e, i'_e, i_h, and i'_h, according to $i_o = i_e + i'_e$ and $i_o = -(i_h + i'_h)$. In Fig. 7(a), it is noted that i_o is composed of the sum of the currents i_e and i'_e, while Fig. 7(b) shows that it is composed of the sum of i_h and i'_h.

From what is described in Section IV and presented in Fig. 8, with load angle $\delta_l = -35°$, it is possible to obtain an optimum voltage angle reducing the current amplitude of both front-end and back-end converters, respectively, converters Se and S_h. The phase difference between the grid and load voltage is shown in Fig. 8(a) and the voltages of the filters capacitors v_{ce} and v_{ch} are presented in Fig. 8(b). The converters' currents are shown in Fig. 8(c) and (d), respectively, converters S_h and S_e. Comparing the presented result, Fig. 8(c) and (d), with Fig. 7, it is noted the diminish of the both front-end and back-end converters's current by optimized load angle.

The set of simulated results obtained for nonlinear case are shown in Figs. 9–11. The explanations for this case are similar to linear results. Fig. 9 shows the compensation of load voltage, grid current with the power factor close to unit and the dc-bus voltage. The converters and circulating currents are presented in Fig. 10. The results form optimized voltage angle are presented in Fig. 11. As the proposed configuration is not isolated, the circulating current will always exist. However, their effects can be minimized making v_o close to v_g by proposed control strategies.

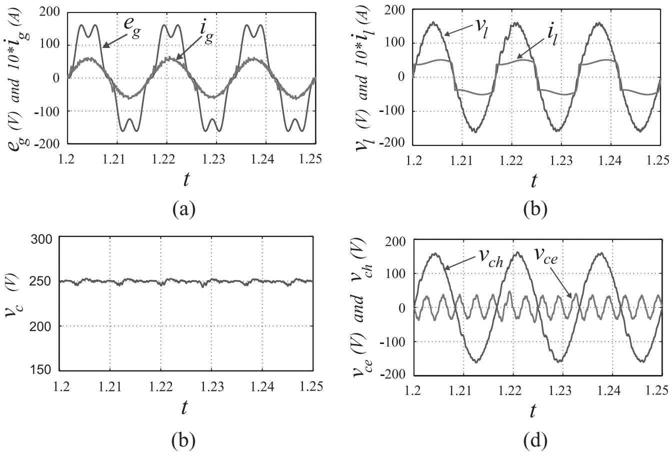


Fig. 9. Simulated results for a nonlinear load: (a) voltage (e_g) and current (i_g) of the grid, (b) voltage (v_l) and current (i_l) of the load. (c) dc-bus voltage (v_c), and (d) voltages v_{ce} and v_{ch}.

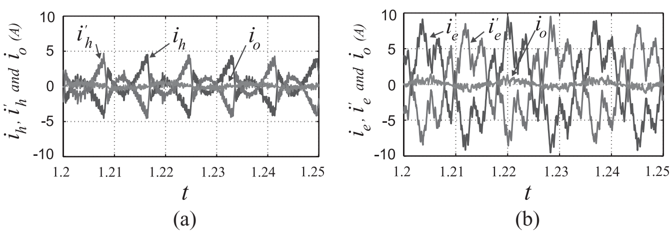


Fig. 10. Simulated results for a nonlinear load: (a) currents of converter S_h (i_h and i'_h) and circulating current (i_o); (b) currents of converter S_e (i_e and i'_e) and circulating current (i_o).

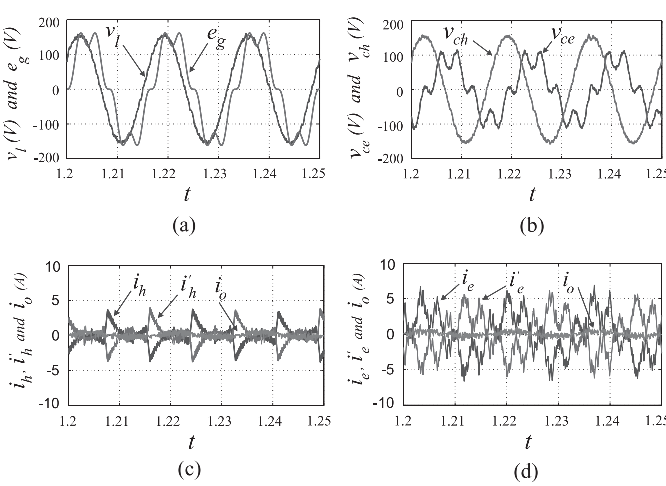


Fig. 11. Simulated results for a nonlinear load with $\delta_l = -35°$: (a) load (v_l) and grid (e_g) voltage, (b) voltages of the filters capacitors v_{ce} and v_{ch}, (c) currents of converter S_h (i_h and i'_h) and circulating current (i_o), (d) currents of converter S_e (i_e and i'_e) and circulating current (i_o).

VIII. Experimental Results

The system in Fig. 1(b) has been tested by using a microcomputer-based system. In the experimental tests, the capacitors were selected as $C = 2200\ \mu$F, and the switching frequency employed was 10 kHz. The selected *PWM* modulation was the general approach (Method A). The system parameters are given by:

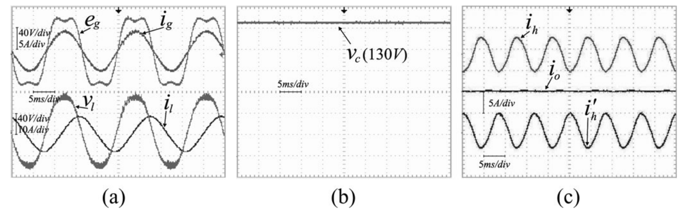


Fig. 12. Experimental results for a linear load: (a) voltage and current of the grid (top); voltage and current of the load (bottom). (b) DC-link voltage. (c) Current i_h (top); circulating current i_o (middle) and current i'_h (bottom).

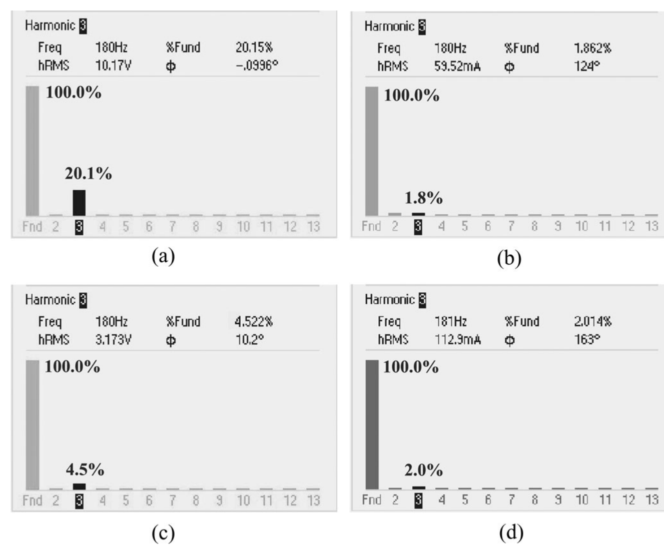
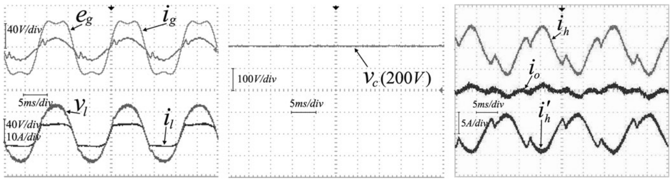


Fig. 13. Spectral analysis of the experimental results for linear load condition: (a) Input voltage—e_g. (b) Input current—i_g. (c) Load voltage—v_l. (d) Load current—i_l.

1) Source frequency of e_g: 60 Hz;
2) Harmonic frequency of e_g: 180 Hz;
3) DC-bus voltage, v_c: 130 V_{dc} and 200 V_{dc};
4) Inductors filters, L_e and L_f: 7 mH;
5) Capacitor filter, C_e: 70 μF;
6) Grid voltage, e_g: 50 V_{rms} and 100 $V_{\mathrm{rms}} \pm 20\%$, respectively, Figs. 12(a) and 14(b)—top;
7) Load voltage, v_l: 50 V_{rms} and 100 V_{rms}, respectively, Figs. 12(a) and 14(b)—bottom;
8) Linear load composed by: $R = 5\ \Omega$ and $L = 63$ mH.
9) Nonlinear load composed by diode bridge rectifier with: $R = 5\ \Omega$ and $L = 75$ mH.

In terms of load types, two sets of experimental results have been collected. The first one is for a linear load condition as observed in Figs. 12 and 13. The other is for nonlinear load condition, composed by diode bridge rectifier, as shown in Figs. 14 and 15.

In Fig. 12(a) are shown the grid voltage e_g and grid current i_g with power factor close to one (top). Additionally, the figure also exhibits the load voltage v_l and load current i_l (bottom). The grid voltage has been obtained from a disturbance voltage source and even in the presence of voltage harmonic in the grid voltage, grid current, and load voltage are sinusoidal. Fig. 12(b) indicates the dc-link voltage control and the Fig. 12(c) shows that even



(a) (b) (c)

Fig. 14. Experimental results for no linear load: (a) voltage and current of the grid (top); voltage and current of the load (bottom). (b) DC-link voltage. (c) Current i_h (top); circulating current i_o (middle) and current i'_h (bottom).

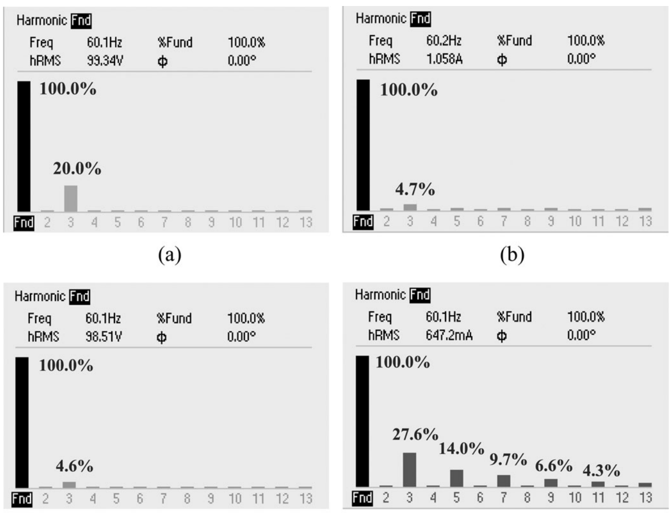


Fig. 15. Spectral analysis of the experimental results for nonlinear load condition: (a) of the input voltage—e_g. (b) of the input current —i_g. (c) of the load voltage—v_l. (d) of the load current—i_l.

without transformer the circulating current i_o is controlled to be close to zero.

The spectral analysis of the presented experimental are shown in Fig. 13. Note that, for the grid voltage [see Fig. 13(a)] the third harmonic (20%) is intentionally added in the voltage waveform, as observed in Fig. 12(a). But even in this case, the grid current in Fig. 13(b) and the load voltage in Fig. 13(c) present low distortion due to the third harmonic component. Fig. 13(d) shows the spectral analysis of load current.

The same set of experimental results is obtained in the case of nonlinear load, as observed in Figs. 14 and 15. As noted in Fig. 14(c), the circulating current i_o is higher than that of linear load due to the presence of harmonic content, but even with this type of load, i_o is considered small.

IX. Conclusion

A suitable control strategy, including the PWM technique has been developed for the proposed UAPF. In this way, it has been shown that the proposed configuration presents low $WTHD$, whose value is, however, higher than that of conventional configuration. This is because of the need to compensate the circulating current i_o via voltage v_o. *Method B*—series (*Method B*—parallel) permits to reduce the WTHD in the series (parallel) converter side, but the $WTHD$ of v_o is higher than that obtained with *Method A*. As there was no need to improve one of the converters side (series or parallel converter), the *Method A* was used to compose the PWM strategy for both simulated and experimental. The proposed transformerless UAPF is controlled according to two proposed PWM techniques objecting the elimination of undesirable circulating current. In terms of the applied control, the converter's currents can be minimized by choosing an adequate load angle δ_l.

From the model obtained, it has been shown that the circulating current can be imposed as close to zero even in the unbalanced case, where the values of filters inductance are different ($L_e \neq L'_e$ and $L_h \neq L'_h$). This means that the controller must define $v_o = v'_{e0} + v_{e0} - v'_{h0} - v_{h0}$ in order to control the i_o closed to zero. So in the converter design, the circulating current i_o is an important variable to be controlled. Because the proposed configuration is transformerless, the circulating current will always exist. But its effects can be greatly minimized from the insertion of v_o close to v_g.

The operation principle, control strategy, steady-state analysis, simulated, and experimental results of the proposed transformerless UAPF were presented under different load conditions and demonstrate adequate harmonic correction and power factor close to one.

Appendix I

Circulating Current

The demonstrations of the circulating current i_o is primarily determined by summing the equations (5)–(8), it becomes

$$v_{e0} - v'_{h0} = v_g + \left(\frac{r_e}{2} + \frac{l_e}{2}p\right) i_e - \left(\frac{r'_h}{2} + \frac{l'_h}{2}p\right) i'_h \quad (42)$$

and subtracting (6) and (7)

$$v_{h0} - v'_{e0} = v_g + \left(\frac{r_h}{2} + \frac{l_h}{2}p\right) i_h - \left(\frac{r'_e}{2} + \frac{l'_e}{2}p\right) i'_e \quad (43)$$

subtracting (42) and (43), then, it has

$$v_{e0}+v'_{e0}-(v_{h0}+v'_{h0}) = -\left[\left(\frac{r_h}{2}+\frac{l_h}{2}p\right) i_h + \left(\frac{r'_h}{2}+\frac{l'_h}{2}p\right) i'_h\right] + v_g + \left(\frac{r_e}{2}+\frac{l_e}{2}p\right) i_e + \left(\frac{r'_e}{2}+\frac{l'_e}{2}p\right) i'_e. \quad (44)$$

Assuming that ($v_o = v'_{e0} + v_{e0} - v'_{h0} - v_{h0}$) and considering the impedances ($Z_e = Z'_e$) and ($Z_h = Z'_h$), the previous equation can be simplified as

$$v_o = \left(\frac{r_e}{2} + \frac{l_e}{2}p\right)(i_e + i'_e) - \left(\frac{r_h}{2} + \frac{l_h}{2}p\right)(i_h + i'_h) + v_g \quad (45)$$

being, v_o, the voltage responsible to cancel the circulating current. Making ($xv_g = v_o$), it becomes

$$0 = \left(\frac{r_e}{2} + \frac{l_e}{2}p\right)(i_e + i'_e) - \left(\frac{r_h}{2} + \frac{l_h}{2}p\right)(i_h + i'_h). \quad (46)$$

From (46), it is noted this relationship will be true if ($i_e + i'_e = 0$) and $[-(i_h + i'_h) = 0]$. Therefore, the circulating current is defined as being $[i_o = i_e + i'_e = -(i_h + i'_h)]$.

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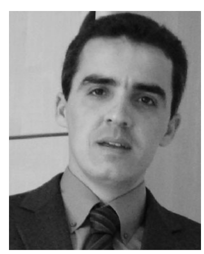

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