Capacitor Balance in a Five-level Based Half-bridge Converter by Use of a Mixed Active-Cell

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***Abstract*—This paper proposes a 5-level half-bridge hybrid converter topology with improved capacitor voltage balance and reduced kVA rating. In order to validate the proposed structure, experimental results are presented. In addition, it is compared with an existing counterpart structure in terms of capacitor voltage oscillation and capacitance size.**

Keywords—half-bridge converter; multilevel converter; power converter; capacitor balancing

I. INTRODUCTION

Multilevel inverters have the capability of reducing output voltage harmonics, and semiconductors voltage stress, especially in medium and high power level. Among these, the well-known multilevel topologies are diode-clamped or neutral-point-clamped (NPC) type [1][2], capacitor-clamped or flying capacitor type [3], and cascaded H-bridge type with separate dc inputs [4]. At the beginning, the main interest was concentrated in three-level configurations [5]-[7] but the increase in application of these converters and improvement of output characteristics led to the development of other level topologies [8]-[15].

Some hybrid topologies presenting five levels at the output phase voltage were introduced in [13]-[15] presenting costs, volume, and control complexity reduction when compared with other topologies. An important feature that should be noticed in these topologies is the presence of devices with different blocking voltage ratings and different frequencies switching. In especial, [15] introduced the half-bridge converter presented in Fig. 1 in its three-phase version. Each half-bridge is composed of a two-level leg and a three-level Active-NPC (ANPC) leg, which allows better distribution of the switching losses in the leg [6]. It can be noticed that the switches in the two-level legs support the full dc-bus voltage rating. Even though, the blocking voltage rating of each switch is in the range from 3.3 kV up to 6.5 kV due to the continuous development of high the power high switching frequency devices such as IGBT (Insulated-Gate Bipolar Transistor) and IGCT (Insulated-Gate Commutated Thyristor) [16][17].

This paper proposes a 5-level half-bridge hybrid converter topology with improved capacitor voltage balance and reduced kVA rating. In order to validate the proposed structure, experimental results are presented. In addition, it is compared with the structure of Fig. 1 in terms of capacitor voltage oscillation and capacitance size.

II. BASIC CONSIDERATIONS

In the topology shown in Fig. 1, some restrictions on the switches driving process can be noticed: switches S_{5a} and S_{6a} present low frequency operation and cannot be turned-on and turned-off simultaneously; S_{2a} and S_{3a} cannot be turned-off simultaneously; at last, S_{xa} and S_{xa} cannot be turned-on simultaneously (such as S_{1a} and S_{7a}). Thus, applying an appropriate modulation, it is possible to obtain five levels at the output phase voltage. It can be noticed that there are eight possibilities to obtain the level 0, four of them to obtain the $+2V_{dc}$, four to obtain $-2V_{dc}$, nine to obtain V_{dc}, and nine to obtain $-V_{dc}$.

Figure 2 shows the four modes used in [15] for one phase during the positive semi-cycle, in which switch S_{5a} is kept ON, while switch S_{6a} is OFF. In Mode 1 (Fig. 2a), switches S_{1a}, S_{2a} and S_{5a} are kept ON, while all other

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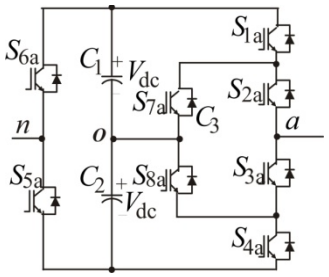


Fig. 1. Half-bridge structure introduced in [15].

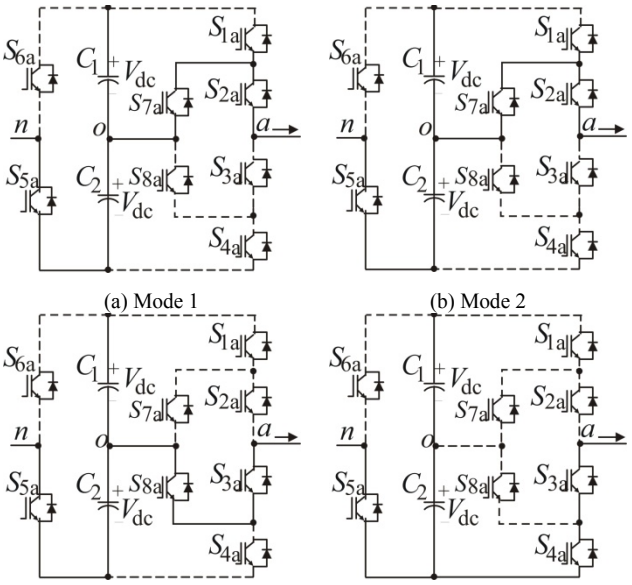


Fig. 2 Modes of operation for the structure in Fig. 1 [15].

switches are OFF; this allow for obtaining the level $2V_{dc}$. Mode 2 (Fig. 2b) and Mode 3 (Fig. 2c) can be used to obtain the level V_{dc}, depending on the switching pattern utilized. In Mode 2, S_{2a}, S_{5a}, and S_{7a} conduct together while all other semiconductors are OFF. Instead, in Mode 3, S_{3a}, S_{5a}, and S_{8a} conduct together while all other semiconductors are OFF.

Mode 2 (Fig. 2b) and Mode 3 (Fig. 2c) can be used to obtain the level V_{dc}, depending on the switching pattern utilized. In Mode 2, S_{2a}, S_{5a}, and S_{7a} conduct together while all other semiconductors are OFF. Instead, in Mode 3, S_{3a}, S_{5a}, and S_{8a} conduct together while all other semiconductors are OFF. Mode 4 (Fig. 2d) generates the zero ("0") level: switches S_{3a}, S_{5a}, and S_{4a} conduct together while all other semiconductors are OFF. During the negative semi-cycle S_{5a} is turned OFF and S_{6a} is kept ON. The operation modes are not shown but can be found in [15].

The positive and negative flux current in the capacitor mid-point unbalances the capacitor voltages and makes them oscillate. In order to avoid these oscillations either the use of six independent sources or an increase in the control complexity is necessary.

III. PROPOSED TOPOLOGY

The half-bridge topology proposed is shown in Fig. 3. A third capacitor is connected in parallel with the active cell (S_{7a} and S_{8a}), in order to improve the control of the capacitor voltages. This concept has been employed in some different topologies [5][8][10] but not in the structure used here. The three-level leg in the topology proposed can be considered as a mixed of ANPC and FC one.

A. Modes of Operation

Consider $C_1 = C_2 = C_3 = C$. The operating modes for phase *a* are shown from Figs. 4(a) to (d). Suppose that ideal v_{c3} is V_d, although, in practice, the value of v_{c3} oscillates around this value. Note that the simultaneous conduction of S_{1a} and S_{7a}, of S_{2a} and S_{3a}, of S_{4a} and S_{8a}, and of S_{7a} and S_{8a} are forbidden situations in order to avoid short-circuiting the capacitors.

Similar to circuit in Fig. 2(a), when S_{1a} is turned ON, phase *a* is connected to the positive DC-bus so that the voltage v_{an} is equal to $+2V_d$. However, in Mode 1 of Fig. 4(a), S_{1a}, S_{2a}, S_{5a}, and S_{8a} are ON, while all other switches are OFF. This way, when $v_{C3}<v_{C1}$, C_3 charges through S_{1a} and D_{8a} and discharges through S_{8a} and D_{1a} when $v_{C3}>v_{C1}$. This allows C_1 and C_3 to be in parallel during these intervals.

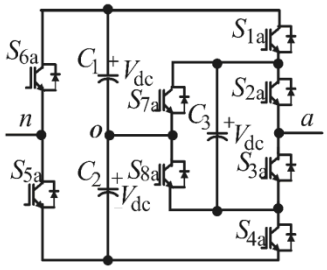


Fig. 3. Proposed Half-Bridge Converter.

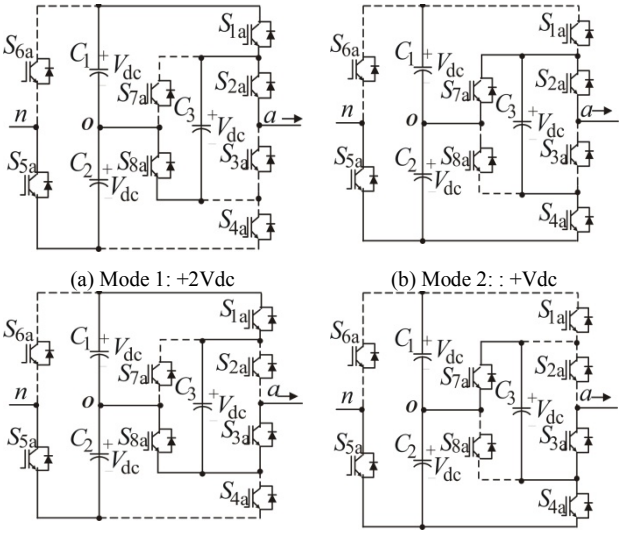


Fig. 4 Modes of operation for the proposed structure.

As in Fig. 2(b), the voltage v_{an} can be made $+V_d$ by turning S_{1a} OFF and turning S_{7a} ON while maintaining S_{2a} ON. when $v_{C3}<v_{C2}$, C_3 is charged by turn on of S_{4a}, as shown in Mode 2 (Fig. 4b). If $v_{C3}>v_{C2}$, C_3 discharges via D_{4a} and S_{7a} can be charged by turn on of S_{4a}, as shown in Mode 2 (Fig. 4b). Another possibility to obtain level $+V_d$ is given in Fig. 4(c), which defines Mode 3. In this case switches S_{1a}, S_{a3}, S_{5a} and S_{8a} are all ON and all other are OFF. When $v_{C3}<v_{C1}$, C_3 charges through S_{1a} and D_{8a}. If $v_{C3}>v_{C1}$, C_3 discharges via

S_{8a} and D_{1a}. As a result, C1 and C3 are connected in parallel during these intervals. Zero voltage is obtained by turning $S_{3a,}$ $S_{4a,}$ $S_{5a,}$ and S_{7a} ON (Mode 4, Fig. 4d). When $v_{C3}<v_{C2}$ these capacitor voltages are made equal by conduction of D7a. If instead $v_{C3}>v_{C2}$ balance is obtained by turning S_{7a} ON.

Other four modes (not shown) are available for achieving the negative semi-cycle, during which S_{6a} is ON and S_{5a} is OFF.

By considering the DC-bus as constant there is not any variation of charge in C_1, C_2 and C_3 during Modes 1 and 4, as shown in Figs. 5(a) and (d). However, although the operation of the half-bridge has been considered as ideal for Modes 2 and 3, there, in fact, a charge of v_{c1} and a discharge of v_{c2} and v_{c3} during Mode 2. Similar there is a charge of increase in the charge of v_{c1} and v_{c3} with and a discharge of v_{c2} during Mode 3. This can be seen from the equivalent circuits in Figs. 5(b) and (c). During the negative flow of the load current, C_1 discharges and C_2 charges and the behavior of C_3 depends on its connection.

The variation in capacitors voltages $v_{c1,}$ v_{c2} and v_{c3} can be calculated for Modes 1 and 3 as shown in the following.

For Mode 2, considering that the capacitors are in equilibrium and that each of them has voltage V_{dc} at the beginning of the mode, it can be shown that

$$v_{c1} = V_{dc} + \frac{I_0 t}{3C} \quad (1)$$

$$v_{c2} = v_{c3} = V_{dc} - \frac{I_0 t}{3C} \quad (2)$$

Therefore, the variation of the capacitor voltage during an interval T_s is given by

$$\Delta v_{c3} = \frac{I_0 T_s}{3C} \quad (3)$$

where T_s is the switching interval and I_0 the output current.

This means that when C3 is connected in parallel to C1, Mode 1 for instance, in a posterior step, the voltage in C_3 is slight different from that in C_1. This difference may originate an inrush current in the switch S_{1a} and diode D_{8a}. Similar to Mode 2, an inrush current may originate when Mode 2 is employed after Mode 3. In order to limit this effect, a small inductor is connected in series with the neutral point, as shown in Fig. 6(a). The operation modes, with the inductor L included, are shown in Fig. 7.

B. PWM Strategy

The control of the proposed structure has been implemented by using the hybrid PWM strategy equivalent to the carrier PWM. In Fig. 8(a) its three-phase version is presented. In this strategy, the references voltages v_a^*, v_b^* and v_c^* are initially declared and can be modified to guarantee the same advantages of the space vector PWM with the ease of implementation of the scalar PWM. The

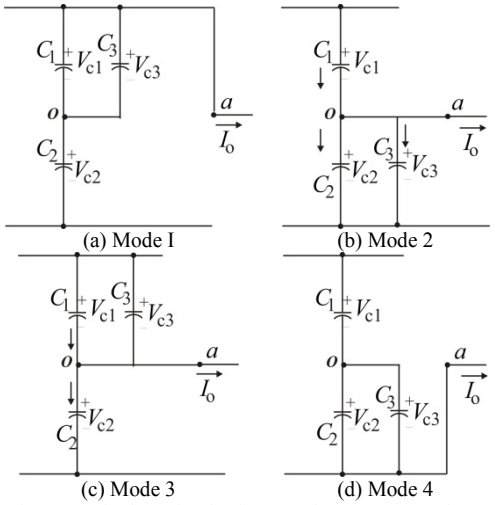


Fig. 5. Equivalent circuits for capacitor C_3 connections.

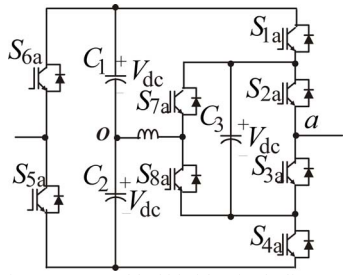


Fig 6. Proposed half-bridge including L

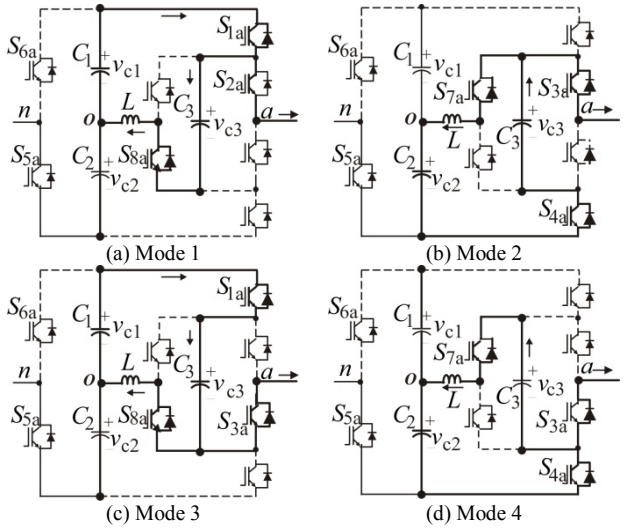
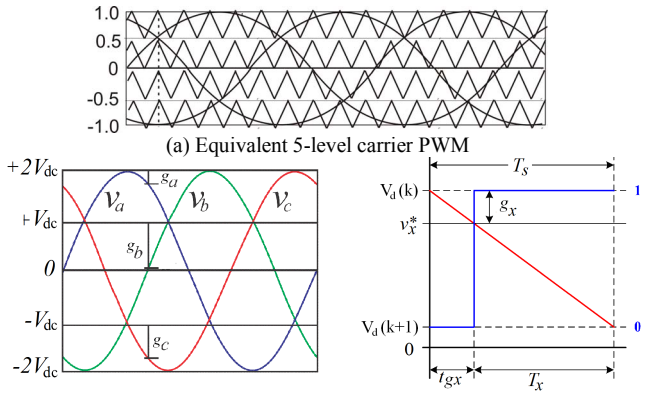


Fig.7. Modes of operation of the half-bridge including L.



(a) Equivalent 5-level carrier PWM

(b) Definition of g_a,g_b and g_c (c) Command pulse

Fig.8. Hybrid PWM.

modified reference voltages $v_a^{*'}, v_b^{*'}$ and $v_c^{*'}$ can be defined from the three-phase references voltages v_a^*, v_b^* and v_c^* as

$$v_a^{*'} = v_a^* + v_h,\ v_b^{*'} = v_b^* + v_h \text{ and } v_c^{*'} = v_c^* + v_h \qquad (4)$$

where v_h is a zero-sequence component, given by

$$v_h = 0.5(g_{\min} + g_{\max} - \frac{V_{dc}}{2}), \qquad (5)$$

In equation (2), $g_{\max} = \max g$, $g_{\min} = \min g$, and $g = \{g_a, g_b, g_c\}$. For defining the values of g_a, g_b and g_c, consider the values of the five converter levels represented by horizontal axes in Fig. 8(b), that is, $V_d(1)$ = +2 V_{dc}, $V_d(2)$ = + V_{dc} , $V_d(3)$ = 0, $V_d(4)$ = - V_{dc} , and $V_d(5)$ = -2 V_{dc} That is, the values of the levels can be generically written as

$$V_d(k) = (1 - \frac{k-1}{2})2V_{dc}, \qquad (6)$$

with k = 1, 2,…,5, for 5 levels. Parameters g_a, g_b and g_c are determined by each difference between the corresponding value of v_a^*, v_b^* and v_c^* and the nearest level which is superior to it (Fig. 8b), that is,

$$if\ (V_d(k) > v_x^* > V_d(k+1)), \text{ then } g_x = V_d(k) - v_x^* \qquad (7)$$

for $x = a, b, c$. In the case, only phase a was considered.

The width of the switches command signals T_a, T_b and T_c, are determined from the principle of triangle equivalence appied to Fig. 8(c), that is,

$$T_x = [1 - \frac{g_x}{V_d}]T_s \qquad (8)$$

For $t_{gx} = \frac{g_x}{V_d}T_s$,

$$If\ (t < t_{px}) \text{ or } (t > 2T_s - t_{px}),\ v_{xn} = value\ of\ V_d\ (k+1)$$

and (9)

$$If\ (t_{px} < t < 2T_s - t_{px}),\ v_{xn} = value\ of\ V_d\ (k).$$

IV. Simulation and Experimental Results

The simulation results of a three-phase structure powered by a bus voltage of 200 V, switching frequency of 5 kHz, mains output frequency of 60 Hz, feeding a load composed of R = 25 Ohms and L=7mH, for an output power of 1.4 kW and modulation index of 0.8 are presented in the following.

Figures 9 and 10 show the output voltage and the voltage ripple in capacitors C1 and C2 obtained with the topology in Fig.1, for different capacitances C and a constant Dc-bus. It can be seen that two capacitances of 2200 µF (Fig. 10) equilibrate the capacitor voltages, reducing the ripple amplitude from 60 V (with C = 200 µF, Fig. 9, top) to 9 V (Fig. 10, top). For the same condition, the output voltage obtained with the structure of Fig. 3, with three capacitances of 200 µF, as shown in Fig. 11(top), produces a voltage ripple amplitude of only 4 V (Fig. 11b). This is quite attractive, mainly because the capacitance value is largely reduced. At same time, the output voltage distortion is improved. These simulations have been carried-out with a constant Dc-link of 200 V and suffer from more distortion when the input capacitances are not large enough. In any case, the capacitor currents assume very high peak values in comparison with the load current, which flow through the switches in conduction. However, these peaks are highly reduced when a damping inductance of 1 µH is connected in series with central point as indicated in Fig. 6. Figure 12 shows the output current, the pole voltage and the current in the three capacitors for C=200 µF. Also, simulation results not shown indicate that the proposed topology produces more switching losses than those produced with the topology of Fig 1 since its switches are more often used.

An experimental set-up was built for testing the proposed half-bridge operation. For comparison, tests have been also realized for the half-bridge topology in Fig. 1. These experimental results are presented in Fig. 13 for C = 2200 µF and in Fig. 15 for C = 200 µF. It can be seen that for C = 2200 µF (as in Fig. 10) there is some unbalance in the voltages with an oscillation of approximately 8V. For C = 200 µF, besides the unbalance and increase in the voltage ripple in the capacitor voltages, the capacitors´ values are not enough to maintain constant the Dc-link voltage thus introducing additional oscillations (ripple around 60V) and distortion in the output current (Fig. 14). For comparison with this unfavorable case, the experimental results for the proposed topology including a damping inductance of 1 µH have been also carried-out for C = 200 µF, as shown in Fig.

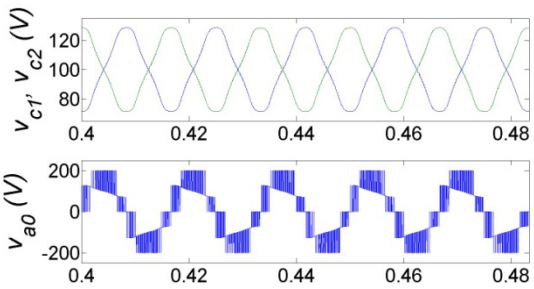


Fig. 9. Pole voltage (top) and capacitor voltages (bottom) for the topology in Fig. 1 [15] with C = 200 µF.

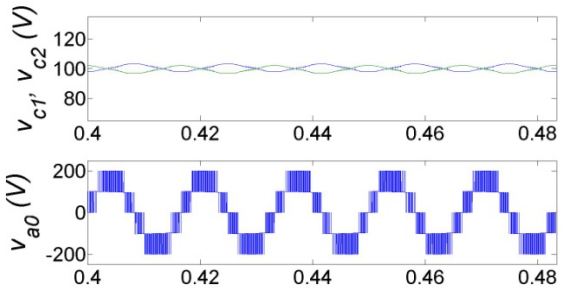


Fig. 10. Pole voltage (top) and capacitor voltages (bottom) for the topology in Fig. 1 [15] with C = 2200 µF.

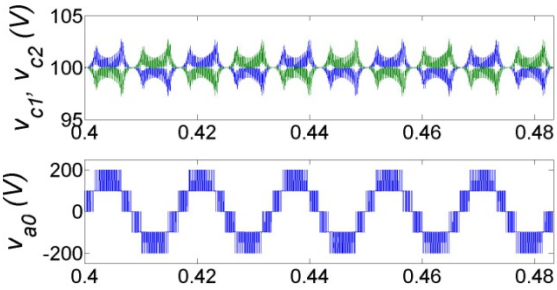


Fig. 11. Proposed topology with C = 200 uF: (a) Pole voltage, and (b) capacitor voltages.

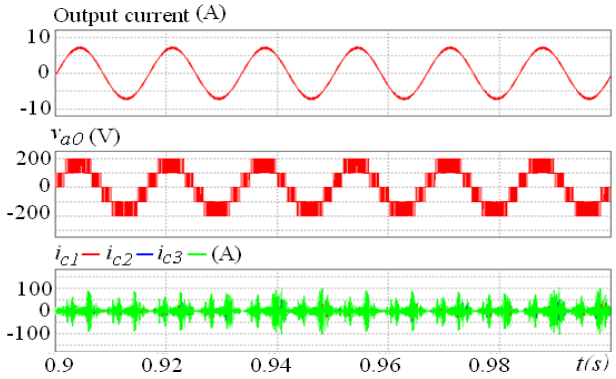
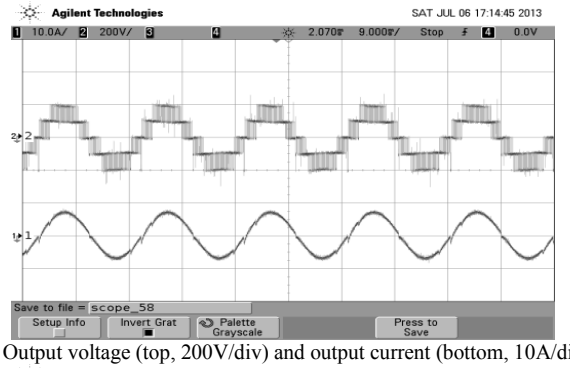
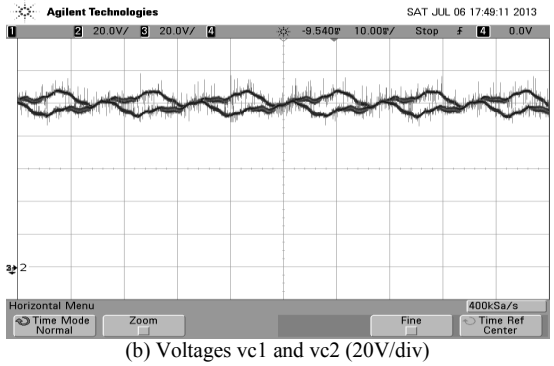


Fig. 12. Proposed topology with a damping inductance of 1 µH included: Output current (top), output voltage (middle) and the current in the three capacitors.

15. Although the Dc-link oscillations are the same as before, balance has been re-established with significant reduction in the voltage ripple of the capacitors, showing that the results

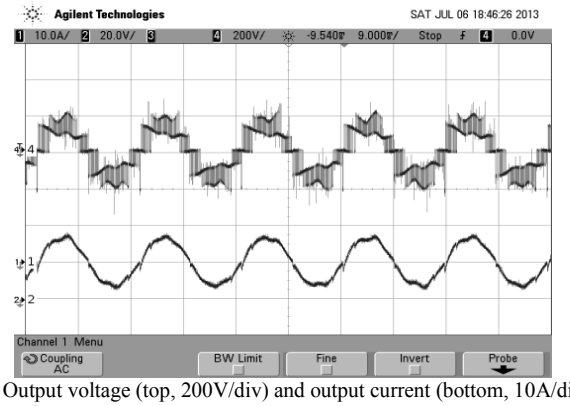


(a) Output voltage (top, 200V/div) and output current (bottom, 10A/div)

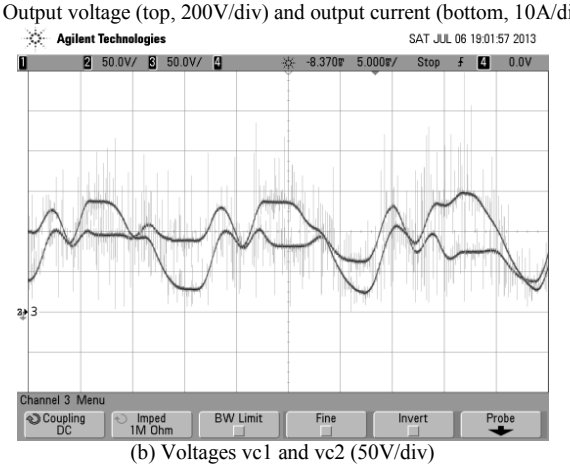


(b) Voltages vc1 and vc2 (20V/div)

Fig. 13. Experimental results for Fig.1 with C= 2200 µF.

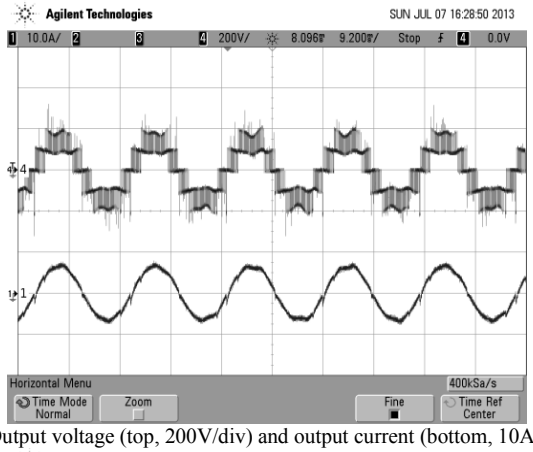


(a) Output voltage (top, 200V/div) and output current (bottom, 10A/div)

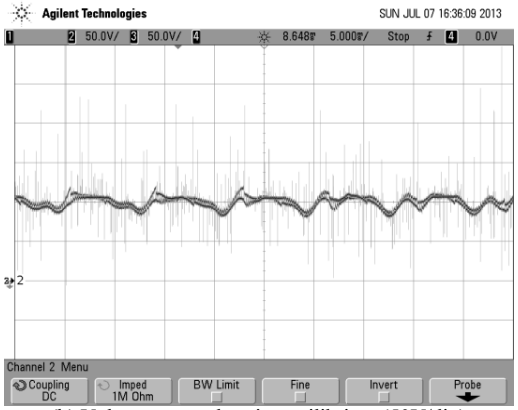


(b) Voltages vc1 and vc2 (50V/div)

Fig. 14. Experimental results for Fig.1 with C= 200 µF.



(a) Output voltage (top, 200V/div) and output current (bottom, 10A/div)



(b) Voltages v_{c1} and v_{c2} in equilibrium (50V/div)

Fig. 15. Experimental results for Fig.6 with C= 200 µF and L=1 µH.

can be improved by an increase in the value of C. Nevertheless, the total capacitance in the circuit will still be significantly reduced when compared to the counterpart topology.

This topology can be easily extended for a three-phase configuration.

V. CONCLUSION

A five-level half-bridge converter topology based on a half-bridge cell is proposed in this paper. The cell is composed of a mixed ANPC leg. The proposed topology was controlled by using a hybrid PWM strategy and compared to a counterpart. Simulated and experimental results showed that the introduction of an additional capacitor to an existing topology needs a much smaller total capacitance to balance the capacitor voltages, to reduce their peak-to-peak ripple and to improve the distortion of phase voltage. However, these results are obtained at the expense of the switching losses, because of an extra switching in the proposed topology.

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